REMARKS

Claims 1, 3 - 8 and 10 - 17 remain active in this application. Claims 2 and 9 have previously been canceled. Approval has been requested for a revision of Figure 1 of the Formal Drawings. Amendment of claims 1, 6, 8 and 12 has been requested to improve clarity and to address criticisms raised by the Examiner. Support for the amendments of the claims is found throughout the application, particularly in Figures 4 and 5 and the description thereof on pages 13 - 16. No new matter has been introduced into the application.

The Examiner has objected to claims 1, 6 and 8 due to several asserted informalities. These objections are respectfully traversed and/or as being moot in view of the amendments requested above.

Specifically, in regard to the words "including" and "received", the objections are moot since the Examiner's suggestions have been adopted. However, it is also respectfully pointed out that "including" and "comprising" are of equivalent import in claim usage notwithstanding the Examiner's assertion that use of the latter is directed by the MPEP (without supporting citation by the Examiner).

In regard to the Examiner's requirement for change of "arrangement" to "controller" "as used in the specification" in claims 1 and 8, it is respectfully submitted that the former term is used throughout the specification; first appearing at page 1, line 10, to comprehend all elements on the chip used for testing of portions of the chip. Therefore, the basis for the requirement asserted by the Examiner is illusory. Moreover, the "BIST controller", as that term is used in the specification, is a subset of BIST elements which, as illustrated in Figure 4, does not include the source of the default test signals. Therefore, the

change in terminology which the Examiner requires would, in fact, be contrary to the usage in both the specification and the claims which is believed to properly emphasize the function of the source of default test signals in combination with other BIST elements in accordance with the invention. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claims 1 and 8 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This ground of rejection is respectfully traversed, particularly as being moot in view of the clarifying amendments made above.

It is respectfully submitted that the Examiner's statement of this rejection as well as the asserted analogy between buffer 206 of Schwarz and the initialization storage module of the invention indicate substantial confusion as to the nature and constitution of the invention and this ground of rejection appears (similarly to the objection discussed above) to be essentially a requirement to conform the claims to a view of the invention which is substantially erroneous. Therefore, before discussing the Examiner's statement of this ground of rejection, a brief summary of the nature of the invention will be provided and which, it is believed, will also be helpful to the Examiner in regard to the rejection based on Schwarz, as will be discussed in detail below.

Built-in self test (BIST) arrangements of many different forms and constitutions are known for performing different tests on various functional sections, such as an embedded memory, of a chip. The types of tests can generally be considered as falling into one of three groups: manufacturing level tests, board level tests and system level tests. Also, in general, external testers can be used for manufacturing level tests and board level tests (e.g. during

manufacture of boards or later service and/or repair) but external testers are not generally available for system level tests which must be performed frequently or upon the occurrence of particular operations such as powering up the system in which a chip requiring testing is installed. It should also be appreciated that storage of signals for use by the BIST structure requires space on the chip and is not justified for manufacturing level and board level tests which are not generally performed after the chip is placed in service, particularly in view of the availability of external testers to supply signals for such tests. Thus, for manufacturing level and board level tests the BIST structure often has a principal function of providing access to signal lines necessary for such tests (see page 5, lines 8 - 11 and page 6, lines 16 - 21). On the other hand, where an external tester is not generally available, as in the case of system level tests (and which are more frequently performed), the inclusion of storage for the test signal patterns on the chip is justified and may be provided by non-volatile storage such as a read only memory (ROM), which may preclude access by an external tester, or small random access memory (RAM); the latter also constituting essentially a further embedded memory which requires testing and which may complicate the test procedure (page 6, lines 3 - 11). Therefore, it is generally preferred to use a register file/instruction storage module 30 (page 6, lines 12 - 16, and page 12, line 30 to page 13, line 4) for manufacturing level and board level testing where an external tester is available for initializing the instruction storage module 30 with a bit string representing the test algorithm and loading instructions for the desired test during the test process (page 6, line 15) even though such an expedient precludes system level test since there no external

tester is available as a source of the test algorithm to initialize the instruction storage module 30. Therefore, there is a basic incompatibility between manufacturing and board level tests (collectively referred to as lower level tests) and system level teats (and other tests referred to as higher level tests) where the test instructions are contained in the BIST arrangement and an external tester is unavailable. This incompatibility is aggravated by the severe constraints on efficiency of chip space usage which, as a practical matter, largely precludes signal connection switching arrangements which may be complex and which must be separately controlled for lower and higher level tests, respectively. Further, while the chip area necessary to accommodate the test instructions for higher level tests may be justified in a BIST arrangement for making such tests, the chip area required to accommodate connection of an external tester must be stringently limited since lower level tests are performed only rarely, if at all, after the chip is placed in service.

To solve this incompatibility consistent with chip area constraints, the invention provides for use of the instruction storage module, preferred for lower level tests, for connection of higher level system test algorithms provided in the BIST arrangement and for internal initialization of the instruction storage module when no initialization signal is available from an external tester or when a particular source of test signals or a particular control signal is discriminated. All that is necessary to perform such a function is to discriminate between lower level tests and higher level tests and to apply an internally generated default initialization signal for higher level tests. The discrimination may be performed efficiently in accordance with the invention by simply determining if a signal applied by an external tester

is present since an external tester will be used for lower level tests but not higher level tests. The remainder of the BIST arrangement operation is not affected (page 15, line 18) and the only operation required is to initialize the instruction storage module when not done in response to signals from an external tester. This operation is completely independent of any structural or operational details of the BIST arrangement and can be performed on any BIST arrangement which uses the much preferred expedient of a file register or instruction storage module.

Therefore, it is respectfully submitted that claims 1 and 8 are not, in fact, incomplete and do not omit essential structural cooperative relationships (although that might be the case if Applicant were to comply with the Examiner's requirement for changing "arrangement" to "controller", traversed above), since it is only necessary that the need for a default initialization signal be determined (e.g. based on availability from an external tester or responsive to a particular control operation or signal) and that such a default initialization signal be generated and applied to the storage means of the BIST. Similarly, it is irrelevant to the accurate characterization and distinction of the invention to describe and particular testing performed by the BIST arrangement. It is also irrelevant to the definition and distinction of the invention whether or not the recited elements of claim 1 are physically placed among the remainder of the BIST elements or merely on a chip having an embedded memory and a BIST arrangement (as is clearly Applicants' intention for construction of the claim recitations); all that is necessary is that the default initialization signal be placed where an externally provided "test signal" would be placed when that "test signal" is not externally applied to the BIST arrangement.

Therefore, it is respectfully submitted that claims 1 and 8 are ,in fact, not incomplete in any way and are entirely sufficient to clearly indicate and convey the intended scope thereof, particularly when amended as requested above. Therefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Claims 1 - 17 have been rejected under 35 U.S.C. §102 as being anticipated by Schwarz without further substantive content beyond mention of the Examiner's general disagreement with remarks previously presented. This ground of rejection is again respectfully traversed. It is also respectfully pointed out that the Examiner's statement of the rejection is ambiguous as to its statutory basis; asserting 35 U.S.C. §102 but referring to "unpatentable", "patentably distinct" and "non-obvious".

Reference is again made to the summary of the invention provided above. In this regard, it is respectfully submitted that some of the Examiner's confusion regarding buffer 206 of Schwarz and the asserted correspondence with the initialization storage module of the present invention may have been occasioned by the invention being described in the specification from the standpoint of extending a BIST arrangement suitable for lower level tests to higher level tests while the arrangement of Schwarz is described from the standpoint of allowing debugging diagnostics (rather than functional testing) to be performed from an external tester. It is respectfully submitted that RAM 102 is being tested in the arrangement of Schwarz while buffer 206 more nearly corresponds to the instruction storage module well-known and preferred in BIST systems.

It is abundantly clear in Schwarz that nothing is applied to buffer 206 (the only storage separately disclosed for test signals to be applied to embedded

memory 102), other than external data and that any internally generated test signals in Schwarz are not applied thereto. No initialization function is described or suggested in Schwarz but, rather, a substantial difficulty of synchronization is admitted (column 4, lines 15 - 32) since the BIST 104 continues to supply address signals during debugging but no solution is provided. By the same token, it is clear that Schwarz does not and is not directed to providing a solution to any incompatibility between test types since the debugging signals must be made fully compatible with addressing provided by BIST 104. Therefore, it is equally clear that Schwarz does not anticipate any claim is the application and no *prima facie* demonstration of anticipation has been made by the Examiner. Moreover, Schwarz does not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness since switching of test signals is performed using multiplexers (which are relatively complex and consume substantial chip space) under the control of an external signal. Therefore, while it is respectfully submitted that Schwarz is not concerned with extending the *types* of tests which can be performed (e.g. *both* higher and lower level tests) but only adding a debugging facility to locate a source of an error detected in whatever testing is otherwise performed, at best, Schwarz does not provide a solution to the problem addressed by the invention or do so by a simple initialization arrangement for an instruction store otherwise present to address the important constraint on minimizing chip space required for the BIST. Therefore, it is respectfully submitted that no *prima facie* demonstration of obviousness has been or can be made based on Schwarz.

Accordingly, it is respectfully submitted that the rejection of claims 1 - 17 is clearly in error

regardless of whether the statutory basis is 35 U.S.C. §102 or §103 and the claims are clearly patentably distinguished from the teachings and/or suggestions of Schwarz. Therefore, it is respectfully requested that the rejection of claims 1 - 17 be reconsidered and withdrawn.

It is also respectfully submitted that the finality of the present office action is premature since it is improper to make an action final where no *prim facie* demonstration of the propriety of grounds of rejection contained therein has been made. Accordingly, it is requested that the finality of the present office action be withdrawn and the above-requested amendments entered as a matter of right. In any case, it is respectfully submitted that entry of the above-requested amendments is well-justified. The above-requested amendments clearly do not raise any new issues since they are directed to clarification consistent with claim 17 for which no amendment is currently requested. The amendments also clearly define patentable distinctions from the prior art applied and place the application in condition for allowance. In the alternative, the entry of the above-requested amendments is in order as providing clarification and thus reducing potential issues and improving form for appeal. Accordingly, entry of the above-requested amendment and favorable action upon reconsideration is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such

action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 of International Business Machines Corporation (East Fishkill).

Respectfully submitted,

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Annotated Marked-Up Drawings

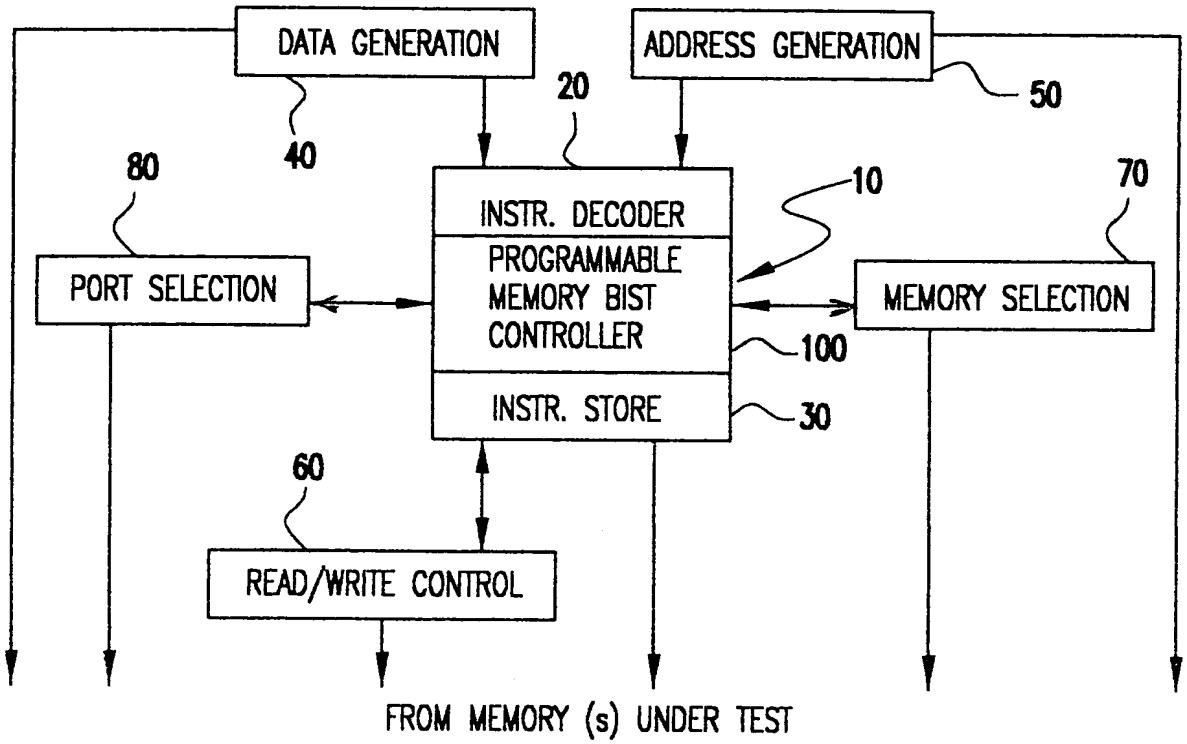

FIG.1